

Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

Claims 1-26 (Canceled)

Claim 27 (New): A semiconductor device comprising:

at least one thin film transistor having a first crystalline semiconductor layer formed on an insulating surface, said first crystalline semiconductor layer including a channel formation region therein; and

a photoelectric conversion element electrically connected to said thin film transistor, said photoelectric conversion element comprising:

a second n-type crystalline semiconductor layer formed on said insulating surface;

a third p-type crystalline semiconductor layer formed on said insulating surface; and

an amorphous semiconductor layer formed on and extending between the second n-type crystalline semiconductor layer and the third p-type crystalline semiconductor layer.

Claim 28 (New): The semiconductor device according to claim 27 wherein said thin film transistor is selected from the group consisting of an amplifying transistor, a selecting transistor and a resetting transistor.

Claim 29 (New): The semiconductor device according to claim 27 wherein said thin film transistor has a gate electrode over said channel formation region with a gate insulating therebetween.

Claim 30 (New): A semiconductor device comprising:

at least one thin film transistor having a first crystalline semiconductor layer formed on an insulating surface, said first crystalline semiconductor layer including a channel formation region therein and at least one p-type impurity region as a source or drain region wherein the p-type impurity region contains both an n-type impurity and a p-type impurity; and

a photoelectric conversion element electrically connected to said thin film transistor, said photoelectric conversion element comprising:

a second n-type crystalline semiconductor layer formed on said insulating surface;
a third p-type crystalline semiconductor layer formed on said insulating surface; and
an amorphous semiconductor layer formed on and extending between the second n-type crystalline semiconductor layer and the third p-type crystalline semiconductor layer,

wherein the third p-type crystalline semiconductor layer contains the same impurities as said p-type impurity region of said one thin film transistor includes.

Claim 31 (New): The semiconductor device according to claim 30 wherein said thin film transistor is selected from the group consisting of an amplifying transistor, a selecting transistor and a resetting transistor.

Claim 32 (New): The semiconductor device according to claim 30 wherein said thin film transistor has a gate electrode over said channel formation region with a gate insulating therebetween.

Claim 33 (New): A semiconductor device comprising:

at least one first thin film transistor having a first crystalline semiconductor layer formed on an insulating surface, said first crystalline semiconductor layer including a channel formation region therein and at least one p-type impurity region as a source or drain region wherein the p-type impurity region contains both an n-type impurity and a p-type impurity;

at least one second thin film transistor having a second crystalline semiconductor layer formed on the insulating surface, said second crystalline semiconductor layer including a channel

formation region therein and at least one n-type impurity region as a source or drain region wherein the n-type impurity region contains an n-type impurity;

a photoelectric conversion element electrically connected to said first and second thin film transistors, said photoelectric conversion element comprising:

a third n-type crystalline semiconductor layer formed on said insulating surface;

a fourth p-type crystalline semiconductor layer formed on said insulating surface; and

an amorphous semiconductor layer formed on and extending between the third n-type crystalline semiconductor layer and the fourth p-type crystalline semiconductor layer,

wherein the third n-type crystalline semiconductor layer contains the same n-type impurity as said n-type impurity region of said second thin film transistor includes, and

wherein the fourth p-type crystalline semiconductor layer contains the same impurities as said p-type impurity region of said first thin film transistor includes.

Claim 34 (New): The semiconductor device according to claim 33 wherein said photoelectric conversion element is directly connected to said first thin film transistor.

Claim 35 (New): The semiconductor device according to claim 33 wherein said photoelectric conversion element is directly connected to said second thin film transistor.

Claim 36 (New): The semiconductor device according to claim 33 wherein said first thin film transistor is selected from the group consisting of an amplifying transistor, a selecting transistor and a resetting transistor.

Claim 37 (New): The semiconductor device according to claim 33 wherein said second thin film transistor is selected from the group consisting of an amplifying transistor, a selecting transistor and a resetting transistor.

Claim 38 (New): The semiconductor device according to claim 33 wherein each of said first and second thin film transistors has a gate electrode over said channel formation region with a gate insulating therebetween.

Claim 39 (New) A semiconductor device comprising:

at least one thin film transistor having a first crystalline semiconductor layer formed on an insulating surface, said first crystalline semiconductor layer including a channel formation region therein; and

a photoelectric conversion element electrically connected to said thin film transistor, said photoelectric conversion element comprising:

a second n-type crystalline semiconductor layer formed on said insulating surface;

a third p-type crystalline semiconductor layer formed on said insulating surface;

an insulating film formed over said second n-type crystalline semiconductor layer and said third p-type crystalline semiconductor layer wherein said insulating film has an opening to expose portions of the second n-type crystalline semiconductor layer and the third p-type crystalline semiconductor layer and a part of the insulating surface between the second n-type crystalline semiconductor layer and the third p-type crystalline semiconductor layer;

an amorphous semiconductor layer formed in the opening of the insulating film so that the amorphous semiconductor layer is in contact with both of the second n-type crystalline semiconductor layer and the third p-type crystalline semiconductor layer.

Claim 40 (New): The semiconductor device according to claim 39 wherein said thin film transistor is selected from the group consisting of an amplifying transistor, a selecting transistor and a resetting transistor.

Claim 41 (New): The semiconductor device according to claim 39 wherein said thin film transistor has a gate electrode over said channel formation region with a gate insulating therebetween.